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09/844,668	04/30/2001	Radhika Thekkath	MTEC004/00US (0121.00US)	8993

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EXAMINER	
PHAM, CHRYSTINE	

ART UNIT	PAPER NUMBER
2192	

DATE MAILED: 06/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/844,668	THEKKATH ET AL.	
	Examiner	Art Unit	
	Chrystine Pham	2192	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9 and 13-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 13-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/03/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to Amendment filed on March 3rd 2005. Claims 10-12 have been canceled. Claims 1, 19-21 have been amended. Claims 1-9, 13-22 are presented for examination.

Response to Arguments

2. Applicant's arguments filed March 3rd 2005 have been fully considered but they are not persuasive.

The Applicant essentially contends that Mann's "use of a separate register to initiate a debug mode does not show or suggest the use of a trace control register to produce synchronization information that includes an operating mode of an embedded processor", "a current process being executed by the embedded processor, and load and store address information" (page 7). First, it is submitted that the single "trace control register" which is claimed to specify a synchronization period as well as to contain fields specifying the operating mode, the current process, and the load and store address information is not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention and to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. FIG.6 and paragraph [1125] of the specification describes trace control register 600 storing the synchronization period PDI_SyncPeriod[2:0]. Nowhere in the specification is the trace control register 600 described to contain fields specifying operating mode of the embedded processor, current process being executed by the processor, or load and store address information. The operating mode of the embedded processor, as described in the specification, is specified in the POM 720 field of a trace record 700 as shown in FIG.7. Another place in which the operating mode is specified is the second trace control register 800 shown in FIG.8. However, nowhere in the specification is the second trace control register 800 described to store or to specify a synchronization information/period. Trace control register 600 and trace control register 800 are clearly shown in FIG.6 and FIG.8 respectively, and disclosed in the specification as two separate and distinct trace control registers with the trace control 600 specifying the synchronization period and the trace control register 800 with fields specifying the operating mode of the processor. Thus, the single "trace control register", as recited in the claim, to specify a synchronization period, operating

mode, current process, load and store address is not disclosed by the specification. Second, in response to Applicant's argument that Mann uses a separate register to initiate a debug mode, as supposed to using a "trace control register" to "specify an operating mode", it is submitted that a debug mode indicates that that the embedded processor is operating under a debug mode, that is to say, the debug mode is the equivalence of the "operating mode" recited in the claims. Furthermore, Mann does not use a register to just initiate a debug mode, but rather, to specify an operating mode of the embedded processor. In col.5:15-21, Mann specifically states that the debug registers 210 include instruction trace configuration register (ITCR) and a debug control status register (DCSR). In col.8:28-60, the DCSR register is disclosed as having a bit field (i.e., STOP) indicating whether the processor 104 (i.e., embedded processor) is in a DEBUG mode (i.e., operating mode). This bit field is used to determine the function of the break request/trace capture signal BRTC and to enable the capture and, subsequently, the generation of trace synchronization information (see *debug control/status register, BRCT* col.6:50-67; see *STOPTX, TRACECLK* col.7:10-18; see *TRACECLK, output data* col.10:37-38). Since the DCSR register is utilized by the trace control circuitry 218 to control and generate trace information, it is clear that the DCSR is the "trace control register". Since the DCSR contains a field indicating the operating mode of the embedded processor, it clearly anticipates the "trace control register" which includes a field "to specify an operating mode of the embedded processor" as recited in the claims.

Applicant further contends that Mann's trace synchronization entry (TCODE=0110, TCODE=0111), which contains the address of the currently executing instruction, does not show or suggest a trace control register with a field specifying a current process being executed. It is submitted that on col.16:1-60, Mann specifically discloses generating trace synchronization information (i.e., trace synchronization entry) containing the current program address (i.e., "current process being executed") (see at least *synchronization entry, TCODE=0110, trace entry, current program address* col.16:1-60). Thus, contrary to Applicant's argument, Mann clearly anticipates "a trace control register with a field specifying a current process being executed" as recited in the claims.

Applicant further contends that Mann fails to show "a trace control register with a field to specify load and store address information" (page 8). It is submitted that, in col.5:20-37, Mann discloses executing read/write (i.e., load/store) operations (i.e., instructions) (see at least *read/write operations, embedded processor device 102, debug registers 210, 206, 218* col.5:20-37). As established above, the trace synchronization entry (TCODE=0110, TCODE=0111) is generated to provide the address of the currently executing instruction (see *trace synchronization entry* col.14:50-53). It is inherent that the address of load/store instruction being executed is provided in the trace synchronization entry. Thus, Mann teaches "a trace control register with a field to specify load and store address information" as recited in the claims.

3. In view of the fore going discussion, rejection of claims 1-9, 13-21 under 35 U.S.C. 102(b) and claim 22 under 35 U.S.C. 103(a) is considered proper and maintained.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 1-9 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement and enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention and to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 1 recites a "trace control register" defining a synchronization period (lines 6-7), "wherein said trace control register includes fields to specify an operating mode of said embedded processor, a current process being executed by said embedded processor, and load and store address information" (lines 8-10). The "trace control register" which is claimed to specify synchronization period, processor operating

mode, current process being executed by the processor and load and store address information is not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention and to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. FIG.6 and paragraph [1125] of the specification describes trace control register 600 storing the synchronization period PDI_SyncPeriod[2:0]. Nowhere in the specification is the trace control register 600 described to contain fields specifying operating mode of the embedded processor, current process being executed by the processor, or load and store address information. The operating mode of the embedded processor, as described in the specification, is specified in the POM 720 field of a trace record 700 as shown in FIG.7. Another place in which the operating mode is specified is the second trace control register 800 shown in FIG.8. However, nowhere in the specification is the second trace control register 800 described to store or to specify a synchronization information/period. Trace control register 600 and trace control register 800 are clearly shown in FIG.6 and FIG.8 respectively, and disclosed in the specification as two separate and distinct trace control registers with the trace control register 600 specifying the synchronization period and the trace control register 800 with fields specifying the operating mode of the processor. Thus, the single "trace control register", as recited in the claim, to specify a synchronization period, operating mode, current process, load and store address is not disclosed by the specification.

Accordingly, claims 2-9 are rejected as claims depending on rejected base claim 1.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-9, 13-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Mann (US 6009270), hereinafter, *Mann*.

Claim 1

Mann teaches a tracing system (e.g., see FIG.1, FIG.2 & associated text), comprising:

an embedded processor (e.g., see *102* FIG.1, FIG.2 & associated text; col.3:65-67), said embedded processor including,

- a processor core for executing instructions (e.g., see *PROCESSOR CORE 104* FIG.1 & associated text; col.4:45-50); and
- trace generation logic (i.e., tracing method) that is operative to periodically generate trace synchronization information (e.g., see *trace synchronization information* Abstract), wherein said trace synchronization information is periodically generated in accordance with a synchronization period (e.g., see *TRACECLK* FIG.2 & associated text; col.7:1-9) defined by at least a part of a trace control register (e.g., see *TRACE CONTROL 218* FIG.2 & associated text; see *TSYNC REGISTER 703* FIG.7 & associated text) .
- wherein said trace control register includes fields to specify an operating mode of said embedded processor (e.g., see *STOPTX* col.7:10-17; see symbol *STOP* TABLE 3 col.8:28:60; see *BRTC* col.6:50-67), a current process being executed by said embedded processor (e.g., see TCODE *0110* TABLE 6 col.13:40-45; see *trace synchronization entry* col.14:50-53; *synchronization entry, TCODE=0110, trace entry, current program address* col.16:1-60), and load and store address information (see at least *read/write operations, embedded processor device 102, debug registers 210, 206, 218* col.5:20-37; *trace synchronization entry, address* col.14:50-53)

Claim 2

The rejection of base claim 1 is incorporated. *Mann* further teaches wherein said synchronization period enables multiple instances of said periodically generated trace synchronization information (e.g., see *200* FIG.3 & associated text) to be stored at one time (i.e., sent or outputted to) in a trace memory (i.e., trace memory included in said embedded processor) (e.g., see *TRACE CACHE 200* FIG.2 & associated text).

Claim 3

The rejection of base claim 2 is incorporated. Claim recites limitations, which have been addressed in claim 2, therefore, is rejected for the same reasons as cited in claim 2.

Claim 4

The rejection of base claim 2 is incorporated. *Mann* further teaches wherein said embedded processor further includes a trace capture block that receives trace data from said trace generation logic (e.g., see *instruction trace capture* col.4:37-41; see *BRKMODE* TABLE 3 col.8:64-66; see *BRTC* col.6:50-67).

Claim 5

The rejection of base claim 4 is incorporated. *Mann* further teaches wherein said trace capture block sends trace data to an off-chip implementation of said trace memory (e.g., see *HOST SYSTEM H* FIG.1 & associated text; see *230* FIG.3 & associated text).

Claim 6

The rejection of base claim 1 is incorporated. *Mann* further teaches wherein said synchronization period is defined by a single field (i.e., containing bit values corresponding to predefined synchronization periods) in said trace control register (e.g., see *TSYNC{6:0}, TCLK{2:0}* TABLE 2 col.8:5-20).

Claim 7

The rejection of base claim 6 is incorporated. Claim recites limitations, which have been addressed in claim 6, therefore, is rejected for the same reasons as cited in claim 6.

Claim 8

The rejection of base claim 7 is incorporated. *Mann* further teaches wherein a first set of said predefined synchronization periods apply to an on-chip implementation of said trace memory (e.g., see *TRACE CACHE 200* FIG.2 & associated text) and a second set of said predetermined synchronization periods apply to an off-chip implementation of said trace memory (e.g., see *200, 230* FIG.3 & associated text).

Claim 9

The rejection of base claim 1 is incorporated. *Mann* further teaches wherein said trace synchronization information includes program counter information (i.e., application space identity information) (e.g., see *COUNTER 701* FIG.7 & associated text; see *current program address* col.16:25-30).

Claim 13

Mann teaches a tracing method, comprising:

Periodically generating trace synchronization information (e.g., see TCODE *0110* TABLE 6 col.13:40-45; see *trace synchronization entry* col.14:50-53; *synchronization entry, TCODE=0110, trace entry, current program address* col.16:1-60) in accordance with a predefined synchronization period (e.g., see *TRACECLK* FIG.2 & associated text; col.7:1-9), said trace synchronization information including program counter information (e.g., see *COUNTER 701* FIG.7 & associated text; see *current program address* col.16:25-30) and information that enables a determination of a characteristic of an operating state (i.e., mode) of a processor (e.g., see *STOPTX* col.7:10-17; see symbol *STOP* TABLE 3 col.8:28:60; see *BRTC* col.6:50-67); and outputting said trace synchronization information to a trace memory (e.g., see *TRACE CACHE 200* FIG.2 & associated text).

Claims 14-18

Claims recite limitations, which have been addressed in claims 1, 2, 9, therefore, are rejected for the same reasons as cited in claims 1, 2, 9.

Claim 19

Mann teaches a computer program product comprising

- computer-readable program code (i.e., computer data signal) for causing a computer to describe an embedded processor (e.g., see FIG.1 & associated text; see claims 10-11 above), said embedded processor including a processor core for executing instructions and trace generation logic that is operative to periodically generate trace synchronization information, wherein said trace

synchronization information is periodically generated in accordance with a synchronization period defined by at least a part of a trace control register (see claim 1); and

- wherein said trace control register includes fields to selectively generate software state information within said trace synchronization information, said software state information being selectable from an operating mode of said embedded processor (e.g., see *STOPTX* col.7:10-17; see symbol *STOP* TABLE 3 col.8:28:60; see *BRTC* col.6:50-67), a current process being executed by said embedded processor (e.g., see TCODE *0110* TABLE 6 col.13:40-45; see *trace synchronization entry* col.14:50-53; *synchronization entry, TCODE=0110, trace entry, current program address* col.16:1-60), and load and store address information (see at least *read/write operations, embedded processor device 102, debug registers 210, 206, 218* col.5:20-37; *trace synchronization entry, address* col.14:50-53); and
- a computer-usable medium (i.e., transmission medium) configured to store the computer-readable program code (e.g., see FIG.2 & associated text).

Claims 20-21

Claims recite limitations, which have been addressed in claims 1, 9, 19, therefore, are rejected for the same reasons as cited in claims 1, 9, 19.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over *Mann* in view of Shagam (US 6311326), hereinafter, *Shagam*.

Claim 22

The rejection of base claim 21 is incorporated. *Mann* does not expressly disclose wherein computer-readable program code is transmitted to said computer over the Internet. However, *Shagam* teaches wherein computer-readable program code (i.e., trace data) is transmitted to said computer over the Internet (e.g., see Abstract; see *400, 402* FIG.3 & associated text; col.1:50-67; col.4:54-56). *Shagam* and *Mann* are analogous art because they are both directed to tracing systems/methods. It would have been obvious to one of ordinary skill in the pertinent art at the time the invention was made to incorporate the teaching of *Shagam* into that of *Mann* for the inclusion of transmitting trace data over the Internet. And the motivation for doing so would have been to facilitate remote online access to and sharing of trace data for debugging software installed on client computers situated in remote locations without imposing significant performance degradation on the client computer system (e.g., interrupting or impairing the client's ability to do business).

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chrystine Pham whose telephone number is 571-272-3702. The examiner can normally be reached on Mon-Fri, 8:30am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on 571-272-3695. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CP
May 30, 2005

TUAN DAM
SUPERVISORY PATENT EXAMINER